

Application No. 10/605,408
Docket No. YOR920000707US2
Amendment dated December 13, 2006
Reply to Office Action of June 13, 2006

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently amended): A method of forming a strained silicon-on-insulator structure, the method comprising the steps of:
 forming a silicon layer on a strain-inducing layer so as to form a multilayer structure, the strain-inducing layer having a different lattice constant than silicon so that the silicon layer is strained during the forming step as a result of a lattice mismatch with the strain-inducing layer; and then
 bonding the multilayer structure to a substrate so that an insulating region is ~~the bonding step being chosen from the group consisting of directly bonding a first insulating layer on and contacting the strained silicon layer of the multilayer substrate to a second insulating layer on the substrate, directly bonding an insulating layer on and contacting the strained silicon layer of the multilayer substrate to a semiconductor layer of the substrate, and directly bonding a first semiconductor layer of the substrate to a second semiconductor layer of the multilayer substrate and separated from the strained silicon layer by~~

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~~an insulating layer, the bonding step resulting in the presence of an insulating region between the strained silicon layer and the substrate, the strained silicon layer directly contacting the insulating region; and then~~

removing the strain-inducing layer to expose a surface of the strained silicon layer and to yield a strained silicon-on-insulator structure comprising the substrate, the insulating region, and the strained silicon layer on the insulating region.

Claim 2 (Previously presented): A method according to claim 1, wherein the substrate is formed of a semiconductor material.

Claim 3 (Previously presented): A method according to claim 1, wherein the strain-inducing layer is formed of a SiGe alloy, and the strained silicon layer is under tensile strain.

Claim 4 (Previously presented): A method according to claim 1, wherein the strained silicon layer is formed by epitaxial growth on the strain-inducing layer.

Claim 5 (Currently amended): A method according to claim 1,

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wherein the insulating region is on the substrate, and the bonding step comprises bonding the insulating region on the substrate to the strained silicon layer of the multilayer structure. ~~the removing step comprises preferentially etching the strain-inducing layer with hydrogen peroxide, hydrofluoric acid, and acetic acid.~~

Claim 6 (Currently amended): A method according to claim 1, wherein the insulating region is on the substrate, the multilayer structure comprises the strain-inducing layer, the strained silicon layer on and contacting the strain-inducing layer, and a second insulating region on the strained silicon layer, and the bonding step comprises bonding the insulating region of the substrate to the second insulating region of the multilayer structure. ~~the bonding step comprises directly bonding the first insulating layer on the strained silicon layer of the multilayer substrate to the second insulating layer on the substrate.~~

Claim 7 (Currently amended): A method according to claim 1, wherein the multilayer structure comprises the strain-inducing layer, the strained silicon layer on and contacting the strain-inducing layer, and the insulating region on the strained silicon layer, and the bonding step comprises bonding

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the insulating region of the multilayer structure to the substrate. ~~the bonding step comprises directly bonding the insulating layer on and contacting the strained silicon layer of the multilayer substrate to the semiconductor layer of the substrate.~~

Claim 8 (Currently amended): A method according to claim 1, wherein the multilayer structure comprises the strain-inducing layer, the strained silicon layer on and contacting the strain-inducing layer, the insulating region on the strained silicon layer, and a semiconductor layer on the insulating region, and the bonding step comprises bonding the semiconductor layer of the multilayer structure to the substrate. ~~the bonding step comprises directly bonding the first semiconductor layer of the substrate to the second semiconductor layer of the multilayer substrate and separated from the strained silicon layer by the insulating layer.~~

Claim 9 (Previously presented): A method according to claim 8, wherein the substrate is formed of a semiconductor material.

Claim 10 (Currently amended): A method according to claim 1, wherein the strain-inducing layer is formed of a SiGe alloy and the removing

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step comprises one or more techniques chosen from the group consisting of
chemical-mechanical polishing, wafer cleaving, and chemical etching selective
to silicon, preferentially etching the strain-inducing layer with hydrogen
peroxide, hydrofluoric acid, and acetic acid.

Claim 11 (Previously presented): A method according to claim 1,
further comprising the step of forming an IC device in the surface of the
strained silicon layer.

Claim 12 (Currently amended): A method according to claim 11,
wherein the step of forming the IC device comprises the steps of forming
source and drain regions in the surface of the strained silicon layer so that the
strained silicon layer defines a channel between the source region and the drain
region, the channel being in direct contact with the insulating region, layer,

Claim 13 (Currently amended): A method of forming a MOSFET
device, the method comprising the steps of:

epitaxially growing a silicon layer on a SiGe layer so as to form a
multilayer structure, the SiGe layer having a different lattice constant than
silicon so that the silicon layer is under tensile strain as a result of a lattice

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mismatch with the SiGe layer; and then

bonding the multilayer structure to a substrate comprising a semiconductor layer, ~~the bonding step being chosen from the group consisting of directly bonding a first insulating layer on the strained silicon layer of the multilayer substrate to a second insulating layer on the semiconductor layer of the substrate, directly bonding an insulating layer on the strained silicon layer of the multilayer substrate to the semiconductor layer of the substrate, and directly bonding the semiconductor layer of the substrate to a second semiconductor layer of the multilayer substrate and separated from the strained silicon layer by an insulating layer~~, the bonding step resulting in the presence of an insulating region between the strained silicon layer and the semiconductor layer of the substrate, the strained silicon layer directly contacting the insulating region; and then

removing the SiGe layer to expose a surface of the strained silicon layer and to yield a strained silicon-on-insulator structure comprising the semiconductor layer, the insulating region, and the strained silicon layer on the insulating region; and then

forming an IC device in the surface of the strained silicon layer.

Claim 14 (Currently amended): A method according to claim 13,

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wherein the substrate comprises the insulating region and the semiconductor layer, and the bonding step comprises bonding the insulating region of the substrate to the strained silicon layer of the multilayer structure. ~~the removing step comprises preferentially etching the SiGe layer with hydrogen peroxide, hydrofluoric acid, and acetic acid.~~

Claim 15 (Currently amended): A method according to claim 13, wherein the substrate comprises the insulating region and the semiconductor layer, the multilayer structure comprises the SiGe layer, the strained silicon layer on and contacting the SiGe layer, and a second insulating region on the strained silicon layer, and the bonding step comprises bonding the insulating region of the substrate to the second insulating region of the multilayer structure. ~~the bonding step comprises directly bonding the first insulating layer on the strained silicon layer of the multilayer substrate to the second insulating layer on the semiconductor layer of the substrate.~~

Claim 16 (Currently amended): A method according to claim 13, wherein the multilayer structure comprises the SiGe layer, the strained silicon layer on and contacting the SiGe layer, and the insulating region on the strained silicon layer, and the bonding step comprises bonding the insulating region of

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the multilayer structure to the semiconductor layer of the substrate. ~~the bonding step comprises directly bonding then insulating layer on the strained silicon layer of the multilayer substrate to the semiconductor layer of the substrate.~~

Claim 17 (Currently amended): A method according to claim 13, wherein the multilayer structure comprises the SiGe layer, the strained silicon layer on and contacting the SiGe layer, the insulating region on the strained silicon layer, and a second semiconductor layer on the insulating region, and the bonding step comprises bonding the semiconductor layer of the substrate to the second semiconductor layer of the multilayer structure. ~~the bonding step comprises directly bonding the semiconductor layer of the substrate to the second semiconductor layer of the multilayer substrate and separated from the strained silicon layer by the insulating layer.~~

Claim 18 (Original): A method according to claim 13, wherein the removing step comprises one or more techniques chosen from the group consisting of chemical-mechanical polishing, wafer cleaving, and chemical etching selective to silicon.

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Claim 19 (Previously presented): A method according to claim 13, wherein the step of forming the IC device comprises forming source and drain regions in the surface of the strained silicon layer so that the strained silicon layer defines a channel between the source region and the drain region, the channel being in direct contact with the insulating region.

Claim 20 (Previously presented): A method according to claim 19, further comprising the step of using the semiconductor layer to form a gate electrode separated from the channel by the insulating region.

Claim 21 (Previously presented): A method according to claim 19, further comprising the steps of forming a gate oxide on the surface of the strained silicon layer, and forming a gate electrode on the gate oxide.

Claim 22 (Previously presented): A method according to claim 19, further comprising the steps of:

using the semiconductor layer to form a first gate electrode separated from the channel by the insulating region;

forming a gate oxide on the surface of the strained silicon layer; and

forming a second gate electrode on the gate oxide;

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wherein the method yields a double-gate MOSFET.

Claim 23 (Previously presented): A method according to claim 13, wherein the SiGe layer is formed of a SiGe alloy having the lattice constant of about 0.2 to about 2 percent larger than the lattice constant of silicon.

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